

2682
PTO/SB/21 (08-00)

MODIFIED

**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

213200.00072

* plus cited references

Application Number 09/920,240

Filing Date 08/01/2001

First Named Inventor Pierte ROO

Group Art Unit 2682

Examiner Name Eugene Yun

Total Number of Pages in This Submission

4 *

Attorney Docket Number MP0039.CIP

ENCLOSURES (check all that apply)

- ☐ Fee Transmittal Form
- ☐ Credit Card Authorization
- ☐ Amendment / Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement with PTO-1449s and cited references
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53

- ☐ Assignment Papers (for an Application)
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Associate Power of Attorney
- ☐ Terminal Disclaimer
- ☐ Request for Refund
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- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENTFirm
or
Individual nameAndrew J. Bateman
Registration No.: 45,573

Signature

Date

08/11/2005

CERTIFICATE OF MAILINGI hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date:

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Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pierte ROO

Application No.: 09/920,240

Filed: August 1, 2001

For: ACTIVE RESISTIVE SUMMER FOR
A TRANSFORMER HYBRID

Examiner: Eugene Yun

Group Art Unit: 2682

Date: August 11, 2005

INFORMATION DISCLOSURE STATEMENTCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

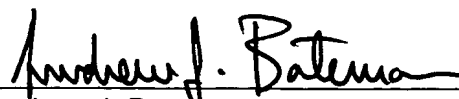
In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449s and to the attached copies of any non-U.S. Patent or literature references cited thereon.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, if deemed necessary, the Commissioner is authorized to charge the IDS fee of \$180.00 to Deposit Account No. 50-1710.

Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

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FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. MP0039.CIP	APPLICATION NO. 09/920,240
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Pierte ROO	
		FILING DATE 08/01/2001	GROUP 2682
DATE SUBMITTED TO USPTO: August 11, 2005			
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)			
*EXAMINER INITIALS			
	Rao, Short Course: Local Area Networks		
	Razavi, Principles of Data Conversion System Design		
	Mano, Digital Logic and Computer Design		
	Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip		
	Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS		
	Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization		
	Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode		
	Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits		
	Lin, et al., A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM		
	Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits		
	Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop		
	Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator		
	Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm		
	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm ²		
EXAMINER		DATE CONSIDERED	
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			